Material Characterization of a High-Dielectric-Constant Polymer–Ceramic Composite for Embedded Capacitor for RF Applications

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ABSTRACT: Embedded capacitor technology can improve electrical performance and reduce assembly cost compared with traditional discrete capacitor technology. Polymer–ceramic composites have been of great interest as embedded capacitor materials because they combine the processability of polymers with the desired electrical properties of ceramics. We have developed a novel nanostructure polymer–ceramic composite with a very high dielectric constant ($\varepsilon_r \approx 150$, a new record for the highest reported ε_r value of a nanocomposite) in a previous work. RF applications of embedded capacitors require that the insulating material have a high ε_r at a high frequency (in the gigahertz range), low leakage current, high breakdown voltage, and high reliability. A set of electrical tests were conducted in this study to characterize the electrical properties of the novel high-ε_r polymer–ceramic nanocomposite developed inhouse. The results show that this material had a fairly high ε_r in the RF range, low electrical leakage, and high breakdown voltage. An 85°C/85% thermal humidity aging test was been performed, and it showed that this novel high-K material had good reliability. An embedded capacitor prototype with a capacitance density of 35 nF/cm^2 was manufactured with this nanocomposite with spin-coating technology. This novel nanocomposite can be used for the integral capacitors for RF applications. © 2004 Wiley Periodicals, Inc. J Appl Polym Sci 92: 2228–2231, 2004

Key words: nanocomposites; dielectric properties; embedded passive; high-K

INTRODUCTION

The fundamental building components for all electronic packaging systems consist of active and passive components on an interconnecting substrate.[1] Resistors, inductors, and capacitors are examples of passive components, which represent a class of electronic components that result in no power gain to an electronic application. For example, in current cellular phone applications, the ratio of passive components to active components is nearly 20:1, and nearly 80% of the circuit board area is occupied by discrete passive components. Conventional discrete components have to be mounted onto a printed wiring board (PWB) or interconnected substrate; thereby, these components have higher parasitics, lower reliability, and large attachment area requirements. Discrete capacitors are used in many applications, such as noise suppression, filtering, tuning, decoupling, bypassing, termination, and frequency determination, but they occupy a substantial geometric surface area; therefore, limitations exist in which capacitors can be placed around the chip periphery.

Integral passives are defined as functional elements either embedded in or incorporated on the surface of an interconnecting substrate. With increased production emphasis toward efficient electronic packaging, integral embedded passive technology may satisfy such demands. The main advantages of embedded passive components include (1) no separate interconnects to the substrate, (2) improved electrical performance, (3) lower cost, and (4) ease of processing. Because of the increased product demands of increased silicon efficiency, package miniaturization, and higher reliability, integral embedded technology will replace discrete electrical components.

Embedded passive component technology is being studied by Georgia Tech's Packaging Research Center in conjunction with the novel concept of a system-on-package (SOP), as shown in Figure 1.[1] SOP utilizes a large organic substrate in which multiple layers contain embedded capacitors, resistors, and inductors. The layers function together through vias that interconnect the component layers and, therefore, make them functional.

Because organic PWBs are used as the substrate for the embedded passive, the processing parameters of all of the related components are of utmost impor-

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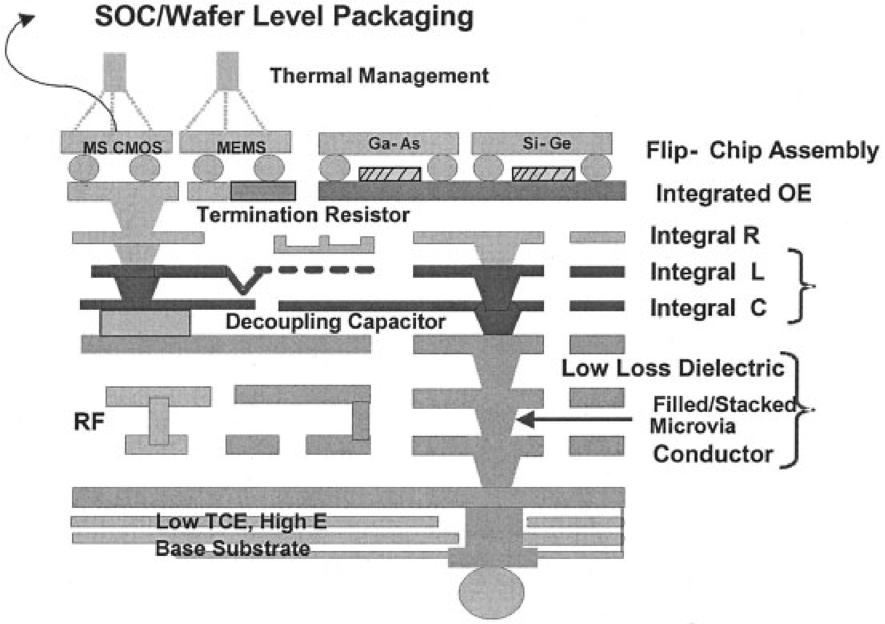

Figure 1 Schematic illustration of the SOP substrate.

tance. The processing conditions for material systems used with the organic substrate are very limited due to the low temperature tolerance of PWBs. The maximum temperature of a PWB before thermal degradation begins at approximately 250°C. To fabricate a high dielectric MCM-L thin film and meet preexisting material specifications, two materials components, a polymeric matrix and a ceramic filler, are used. The polymeric matrix (epoxy) possesses low processing temperatures applicable for PWB applications but has an inherently low dielectric constant (ε_r) value of around 3–4. The ceramic fillers, such as barium titanate (BT) and lead magnesium niobate–lead titanate (PMN–PT), have inherently high ε_r values of 3,000 and 19,316, respectively, making them suitable for decoupling applications. Therefore, a hybrid composite utilizes the processability of the organic polymer matrix and the high dielectric properties of the ceramic fillers. Rao et al. obtained a 70% ceramic volume loading, resulting in a ε_r value of 110.[2] Such a processing method is compatible with MCM-L technology and is easily processed, resulting in associated low costs. In addition, a metal chelating agent, metal acetylacetonate (acac), is used to further increase the ε_r of the epoxy material. On dissociation of the metal acac, charges are released into the polymer matrix, thereby resulting in increased polarization behavior and high-ε_r properties.

The embedded capacitors are fabricated into a parallel-plate configuration, where the capacitance is calculated with the following equation:

$$C = \frac{\varepsilon_o \varepsilon_r A}{t} \tag{1}$$

where C is the capacitance (F), ε_o is the relative permittivity (8.854×10^{-12} F/m), ε_r is the dielectric constant, A is the electrode area, and t is the thickness of the dielectric medium.

According to Rector, some of the many challenges and difficulties encountered with integral capacitors are a low breakdown voltage, high leakage current, and poor simultaneous switching noise (SSN).[3] The power supply noise, due to large numbers of simultaneously switching circuit elements, has been a concern for a long time. The round-trip time-of-flight delay (series inductance) increases as the decoupling capacitor is placed away from the chip.[4] A decoupling capacitor can be used to minimize the on-chip noise or SSN by direct placement close to the chip, which minimizes the interconnect distance and lowers the parasitics. Breakdown voltage is the voltage value at which the material can no longer support the direct current (dc) voltage passing through the material medium. The leakage current is defined as the dc current per unit area passing through the material under a certain dc bias.[5]

EXPERIMENTAL

In the previous work,[2] a high-K epoxy system was developed by with a bisphenol A epoxy resin (DER 661 from Dow Chemical and 5 wt % Co(III) acac as the curing catalyst. The reported ε_r of this high-K epoxy was 6.4, which was 80% higher than the inherent ε_r value of DER661 with the normal curing catalyst. With this high-K epoxy and the combination of two ceramic fillers, PMN–PT (from TAM Ceramics) and $BaTiO_3$ (BT-16 from Cabot Inc.), polymer–ceramic composites

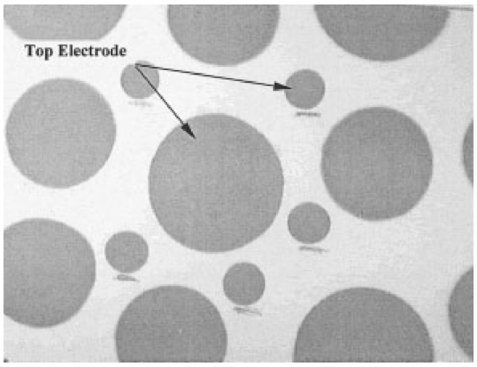

Figure 2 Prototype of capacitors fabricated by thick film technology.

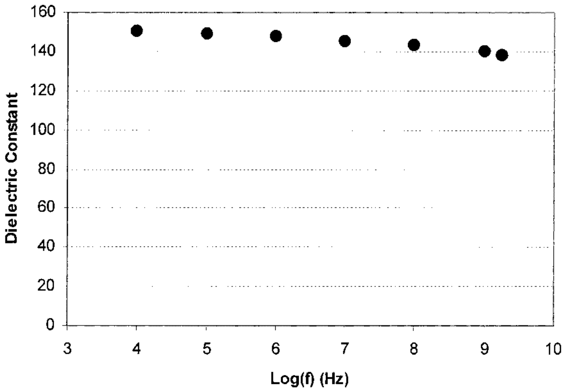

Figure 3 ε_r values of composite I at different frequencies.

were developed by a ball-milling process. The average particle radius of PMN–PT and $BaTiO_3$ were 0.9 and 0.050 μm, respectively. The volume ratio of PMN–PT and $BaTiO_3$ was chosen as 4:1 to obtain the highest possible packing density. To achieve a good dispersion of the ceramic fillers in the epoxy matrix, a phosphate ester (Byk-w 9010, Dow Chemical) was used as the surfactant. A sample (composite I) containing 85 vol % filler loading was ball-milled for approximately 1 day at a speed of 220 rpm to obtain a good particle dispersion.[6] The viscosity of the sample was adjusted by the addition of solvents (*N*-methylpyrrolidone). To obtain the ε_r values for the epoxy system, a prototype of the embedded capacitors were fabricated (see Fig. 2). Capacitance measurements were taken with a HP 4263A LCR meter at 10 kHz. ε_r values were calculated from the capacitance data with eq. (1). ε_r of composite I was calculated as 150.

A set of electrical tests was conducted to characterize the high-K epoxy–ceramic nanocomposite. First, ε_r was measured in the frequency range 10 kHz–1.8 GHz with a HP 4291A RF impedance/material analyzer. Second, we measured the leakage current with an amperemeter (or ampmeter) by connecting the sample with two electric microprobes. Third, an adjustable dc power supply was used to measure the breakdown voltage of the composite. Fourth, a programmable hot plate was used with the HP 4263A LCR meter to characterize the thermal tolerance of a typical capacitor with a thickness of 3.75 μm. The *thermal tolerance* is defined as the relationship between the capacitance and the temperature. Finally, capacitance was measured for the same capacitor after an 85°C/85% thermal humidity (TH) aging test.

RESULTS AND DISCUSSION

Figure 3 shows the ε_r values of the composite at different frequencies. The decrease in ε_r was less than 10% from 10 kHz to 1.8 GHz. This outstanding feature of low loss makes composite I suitable for the production of an embedded decoupling capacitor for RF applications.[7]

Figure 4 shows the leakage current of composite I when the thickness of the material was 3.75 μm. The leakage current was less than 2nA/m^2 under a 6-V dc bias, and it leveled off at higher dc bias values. The leakage current of composite I can fulfill the requirements for embedded capacitor applications.

Figure 5 shows the capacitance density change of an embedded capacitor prototype with composite I as insulating material at different temperatures. Basically, ε_r increased from 35 to 38.4 nF/cm^2 when the temperature increased from 25 to 155°C, which was an increase of less than 10%. However, it was difficult to obtain the ε_r change according to thermal loading, because it was difficult to exclude the geometry change of the capacitor.

Figure 6 shows the capacitance density of the previous capacitor a certain time after the 85°C/85% TH aging test. The capacitance increased in the first 24 h after the 85°C/85% TH aging test; after that, the temperature had no affect on the capacitance. We believe that moisture absorption played an important role in

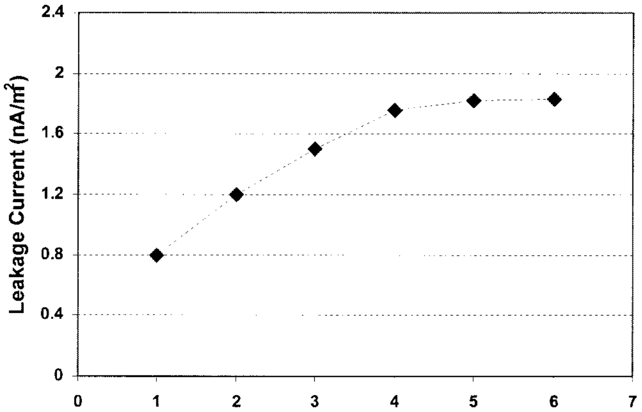

Figure 4 Leakage current of composite I.

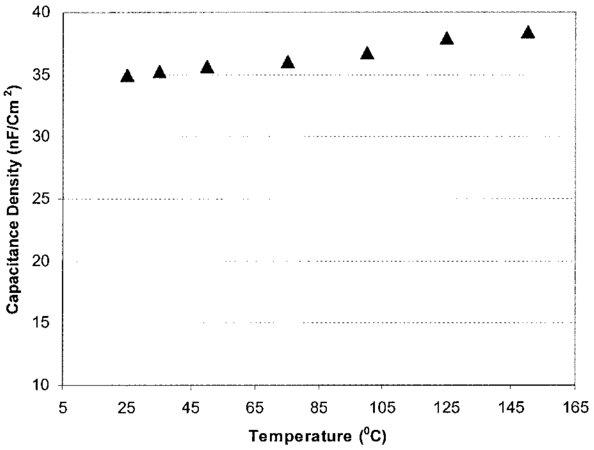

Figure 5 Capacitance densities of composite I (3.75 μm thick) at different temperatures.

the initial capacitance increase. The moisture absorption became saturated after 24 h. Figure 7 shows the moisture absorption of composite I under the 85°C/85% conditions. Because the total moisture absorption was less than 2%, the capacitance density increased by 2.5% 1000 hr after the 85°C/85% TH aging test. There was no electrical failure during the 85°C/85% TH aging test.

The breakdown voltage of composite I was higher than 1.7×10^7 V/m, which is high enough for the composite to serve as an insulating material for an embedded capacitor.[3]

CONCLUSIONS

With an in-house developed high-K epoxy as the matrix, composite I, with a ε_r value of 150, was developed at 85 vol % ceramic loading. A set of electrical and reliability tests were conducted to characterize the physical properties of composite I. Composite I had a stable ε_r in a wide frequency range (10 kHz–1.8 GHz), a very high breakdown voltage, and a small leakage current. An embedded capacitor prototype was fabricated with composite I, and this prototype achieved a capacitance density of 35 nF/cm^2. The capacitance density change of this capacitor was less than 10% from 25 to 155°C. In addition, composite I had a relatively small moisture absorption ($< 2\%$), which led to a stable capacitance after the 85°C/85% TH aging test. There was no electric failure after 1000 h at the 85°C/85% TH aging test. As such, composite I may be a very good material candidate for embedded capacitors in RF applications.

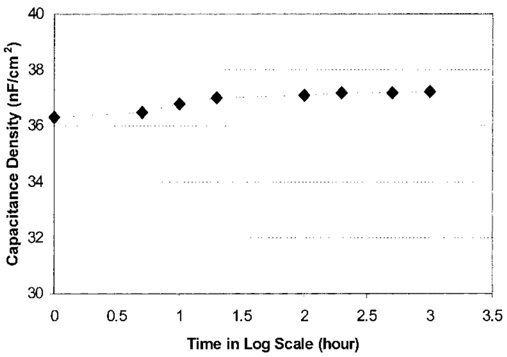

Figure 6 Capacitance densities of composite I (3.75 μm thick) after the 85°C/85% TH aging test.

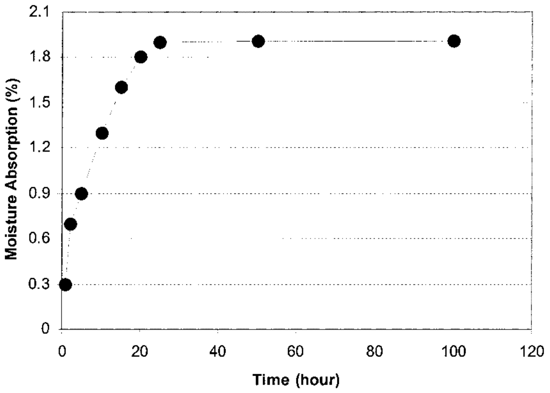

Figure 7 Moisture absorptions of composite I (3.75 μm thick) at the 85°C/85% TH conditions.

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